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TEST ASSEMBLY FOR INTEGRATED CIRCUIT PACKAGE

Background of the Invention

1 Field of the Invention

The present invention generally relates to a semiconductor device test board and a method for testing an integrated circuit (IC) package, and more particularly to a test board and a testing method for an integrated circuit package having solder bumps.

2. Description of the Related Art

As electronic devices have become more smaller and thinner, the velocity and the complexity of chip become more and more higher. Accordingly, a need has arisen for higher package efficiency. To meet the need, integrated circuit packages using solder bumps as external connection terminals have been developed by the semiconductor industry.

The above described integrated circuit package are subjected to various tests such as a solder joint reliability test with the solder bumps connected to a test board.

A conventional semiconductor device test board 100, shown in FIG. 1, includes a plurality of contact pads 110 as denoted with A1 to U21 in FIG. 1 and a plurality of test pads 120 as denoted with 1 to 17 in FIG. 1. The contact pads 110 and the test pads 120 are all interconnected by conductive traces 130. The contact pads 110 are designed to be connected to the solder bumps (not shown) provided on an integrated circuit package to be tested. Accordingly, when the integrated circuit package is mounted on the test board 100, the solder bumps provided on the integrated circuit package are connected by reflow soldering to the contact pads 110 of the test board 100. Thereafter, the solder joint reliability test is conducted by using an ohmmeter to determine whether the electrical connections are complete in such a connected state. If the measured resistance of the major test pads S and E is larger than a predetermined value, it means that at least one solder joint fails in the test. In this situation, every pair of test pads (such as 1/2, 2/3..... illustrated in FIG. 1) will be probed to measure their resistance so as to find out which group of solder joints fails in the test.

Then, a failure analysis is conducted to find out which solder joint fails in the test. First, the integrated circuit package mounted on the test board is embedded in a piece of resin, and then a grinding operation is conducted to expose the cross section of the solder joints. Finally, a scanning electron microscope (SEM) is utilized to observe the cross section.

It is noted that the contact pads 110 connected between one pair of test pads 120 are randomly distributed in different rows. Since the grinding operation must be conducted from outer rows to inner rows, there is a problem that the SEM failure analysis becomes a time-consuming process when the test board 100 shown in FIG. 1 is used.

5 Consequently, there is a need existed for a semiconductor device test board and a method for testing an integrated circuit package which overcomes, or at least reduces the above-mentioned problems of the prior art.

Summary of the Invention

10 It is an object of the present invention to provide a test assembly including a package substrate and a test board for an integrated circuit package and a method of testing an integrated circuit package which can significantly reduce the time for conducting the SEM failure analysis.

15 To achieve the above listed and other objects, the package substrate of the present invention is provided with a plurality of first contact pads linked in a first daisy chain pattern, and the test board of the present invention has a plurality of second contact pads linked in a second daisy chain pattern and a plurality of test pads wherein all of the second contact pads are divided into a plurality of groups each connected to one pair of test pads, and all of the second contact pads in any group are arranged in a line.

20 According to the present invention, the testing method comprises the following steps: (a) mounting an integrated circuit package with the above mentioned substrate on the test board by reflowing solder bumps provided on the integrated circuit package to the second contact pads of the test board, and (b) performing an electrical test after conducting the mounting step.

25 Since the first daisy chain pattern is complementary to the second daisy chain pattern, all of the second contact pads in any group are in a series electrical connection to one another through the first and second daisy chain patterns. In step (b), all of the second contact pads in any group form a closed circuit when the corresponding pair of test pads is probed. Furthermore, the test board includes a pair of major test pads such that all of the second contact pads form a closed circuit when the pair of major test pads is probed.

30 It is noted that, when one pair of the test pads is probed, all of the second contact pads in the corresponding group are arranged in a line. Since the grinding operation of the SEM failure analysis is conducted from outer rows to inner rows, the time for conducting the SEM

failure analysis is significantly reduced when the package substrate and the test board of the present invention are used.

Brief Description of the Drawings

Other objects, advantages, and novel features of the invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings.

FIG. 1 is a top plan view of a conventional semiconductor device test board;

FIG. 2 is a top plan view of a package substrate according to one embodiment of the present invention;

FIG. 3 is a top plan view of a semiconductor device test board according to one embodiment of the present invention; and

FIG. 4 illustrates an integrated circuit package with the substrate of FIG. 2 mounted on the test board of FIG. 3.

Detailed Description of the Preferred Embodiment

In the IC package testing method according to the present invention, the IC package (not shown) has a package substrate 200 (see FIG. 2) specially designed for solder joint reliability test. The package substrate 200 is of the same size and shape as the substrates for mass production. The package substrate 200 is provided with a plurality of first contact pads 210 linked in a first daisy chain pattern. The package substrate 200 is a ball grid array (BGA) substrate.

The test board 300 according to one embodiment of the present invention, shown in FIG. 3, includes a plurality of second contact pads 310 as denoted with A1 to U21 in FIG. 3 and a plurality of test pads such as test pads N to N5 in FIG. 3. All of the contact pads 310 are linked in a second daisy chain pattern and divided into a plurality of groups each connected to one pair of test pads wherein all of the second contact pads 310 in any group are arranged in a line. For example, the contact pads A1 to U1 are belonged to the same group connected to the test pads N and W5. As described below, the contact pads 310 are designed to be connected to the solder bumps provided on an IC package to be tested.

Now a testing method according to one embodiment of the present invention will be described, which is performed on an IC package with the above mentioned substrate 200 using the test board 300 of the above structure.

First of all, a mounting step is performed for mounting the IC package on the test board. Mounting is performed after the solder bumps formed on the IC package are aligned with the second contact pads of the test board. Then, by reflowing the solder bumps to the second contact pads of the test board, the IC package is fixed to the test board. When the IC package
5 is mounted as described above, the first contact pads 210 are electrically connected to the corresponding second contact pads 310 through the solder bumps.

Then, after conducting the mounting step, the probes of an ohmmeter are connected to the test pads 320 of the test board 300, and an electrical test is performed to determine whether the electrical connections are complete. Since the first daisy chain pattern is complementary
10 to the second daisy chain pattern, all of the second contact pads 310 in any group are in a series electrical connection to one another through the first and second daisy chain patterns when the package substrate 200 is mounted on the test board 300. When one pair of the test pads 320, e.g., the test pads N/W5 shown in FIG. 3, is probed, all of the second contact pads 310, i.e., the contact pads A1 to U1, in the corresponding group connected to the test pads
15 N/W5 form a closed circuit. Therefore, when the measured resistance of the major test pads S and E is larger than a predetermined value, it means that at least one solder joint fails the test. In this situation, every pair of test pads (such as N/W5, N1/W4..... illustrated in FIG. 4) will be probed to measure their resistance so as to find out which group of solder joints fails in the test.
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Then, a failure analysis is conducted to find out which solder joint fails in the test. First, the integrated circuit package mounted on the test board is embedded in a piece of resin, and then a grinding operation is conducted to expose the cross section of the solder joints. Finally, a scanning electron microscope (SEM) is utilized to observe the cross section.
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It is noted that, in the test board 300 according to one preferred embodiment of the present invention, all of the second contact pads in any group are arranged in a line. Since the grinding operation must be conducted from outer rows to inner rows, the time for conducting the SEM failure analysis is significantly reduced when the package substrate and the test board of the present invention are used.
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The IC package testing method according to the present invention may be utilized to test the reliability of the solder joints under environmental stress conditions such as temperature cyclic test, three point bending test, vibration test, and drop test.

Although the invention has been explained in relation to its preferred embodiments as described above, it is to be understood that many other possible modifications and variations can be made without departing from the spirit and scope of the invention as hereinafter claimed.